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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RILEY, SHAWN	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/519,306	SICARD, THIERRY	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *dec04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 21 is objected to under 37 C.F.R. 1.75(a) because of the following informalities: "+claim". Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-23 are rejected under 35 U.S.C. §102(a) as being fully anticipated by Castelli et al (U.S. Patent 6,300,749). Castelli et al shows,[1] (in, e.g., the(ir) figures 6 and corresponding disclosure)

As to claim 1. A low drop-out voltage regulator comprising: transistor means (M13/18/M_2 see, e.g., column 5 lines 2-19) for receiving a reference voltage (from 0TA through buffer 4) and in dependence thereon producing a regulated output voltage (OUT); an output stage

1 Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim and may be repeated for convenience of the applicant/examiner. Bolded words/phrases indicate rejected material based 112 paragraph rejections. Underlined words/phrases indicate objected to material.

(M_2/M22/M13/18) for coupling to a load; first direct current (DC) control loop means ($3/V_{REF}/R_1/R_2$) coupled to the transistor means for providing a dominant pole; and second direct current (DC) control loop means (M_2/A/M22) for providing a non-dominant pole, whereby stability of operation may be obtained with a lower load capacitance.

As to claim 2. The low drop-out voltage regulator as claimed in claim 1 wherein the control loop means comprises: differential amplifier (OTA) means having an output coupled to the transistor means; and voltage divider means (R_1/R_2) coupled between the voltage regulator output and a first input of the differential amplifier means.

As to claim 3. The low drop-out voltage regulator as claimed in claim 2 wherein the control loop means further comprises: voltage reference means coupled between the voltage regulator output and a first input of the differential amplifier means.

As to claim 4. The low drop-out voltage regulator as claimed in claim 1 wherein the output stage comprises a low impedance (output is low impedance) output.

As to claim 5. A low drop-out voltage regulator as claimed in claim 1 wherein the second direct current (DC) control loop means is coupled to the voltage regulator output and first direct current (DC) control loop means (all loops are coupled together electrically).

As to claim 6. A low drop-out voltage regulator as claimed in claim 1 wherein the second direct

current (DC) control loop means has a unity direct current (DC) gain (there is a unity gain in the second control loop).

As to claim 7. The low drop-out voltage regulator as claimed in claim 1 wherein the transistor means comprises a cascode transistor arrangement (M13 is in cascade with M_2).

As to claim 8. The low drop-out voltage regulator as claimed claim 1 wherein the output stage comprises a cascode transistor arrangement (M_2 is in cascade with M22).

As to claim 9. The low drop-out voltage regulator as claimed in claim 1 wherein the output stage comprises a P-type transistor (18 is a p-type).

As to claim 10. The low drop-out voltage regulator as claimed in claim 9 wherein the P-type transistor is a PMOS transistor (18 is a PMOS).

As to claim 11. The low drop-out voltage regulator as claimed in claim 1 wherein the transistor means comprises at least part of the second direct current (DC) control loop means (these are connected electrically).

For method claims 12-22, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Therefore the previous rejections based on the

apparatus will not be repeated.

12. A method for low drop-out voltage regulation comprising: providing transistor means receiving a reference voltage and in dependence thereon producing a regulated output voltage; providing an output stage for coupled to a load; providing first direct current (DC) control loop means coupled to the transistor means for providing a dominant pole; and second direct current (DC) control loop means and providing a non-dominant pole, whereby stability of operation may be obtained with a lower load capacitance.

13. The method for low drop-out voltage regulation as claimed in claim 12 wherein the control loop means comprises: differential amplifier means having an output coupled to the transistor means; and voltage divider means coupled between the voltage regulator output and a first input of the differential amplifier means.

14. The method for low drop-out voltage regulation as claimed in claim 13 wherein the control loop means further comprises: voltage reference means coupled between the voltage regulator output and a first input of the differential amplifier means.

15. The method for low drop-out voltage regulation as claimed in claim 12 wherein the output stage comprises a low impedance output.

16. The method for low drop-out voltage regulations claimed in claim 12 wherein the second direct current (DC) control loop means is coupled to the voltage regulator output and first direct current (DC) control loop means.

17. The method for low drop-out voltage regulation as claimed in claim 12 wherein the second direct current (DC) control loop means has a unity direct current (DC) gain.

18. The method for low drop-out voltage regulation as claimed in claim 12 wherein the transistor means comprises a cascode transistor arrangement.

19. The method for low drop-out voltage regulation as claimed in claim 12 wherein the output stage comprises a cascode transistor arrangement.

20. The method for low drop-out voltage regulation as claimed in claim 12 wherein the output stage comprises a P-type transistor.

21. The method for low drop-out voltage regulation as +claimed in claim 20 wherein the P-type transistor is a PMOS transistor.

22. The method for low drop-out voltage regulation as claimed in claim 12 wherein the transistor means comprises at least part of the second direct current (DC) control loop means.

As to claim 23. An integrated circuit comprising the low drop-out voltage regulator of claim 1 (this circuit is integrated).

Allowable Subject Matter

3. No claims are allowable over the prior art of record.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Karl Easthom who can be reached at 571.272.1989. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number **571-273-8300**. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

October 06

Shawn Riley
Primary Examiner